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10/735,507	12/11/2003	Harald Jager	5367-62	5320

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COHEN, PONTANI, LIEBERMAN & PAVANE
Suite 1210
551 Fifth Avenue
New York, NY 10176

EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,507	JAGER ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,21-23 and 26* is/are rejected.

7)☒ Claim(s) *13-20,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/5/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 6 March 2006. Claims 1-26 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 9-11, 21-23 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Maeda et al. (7,023,019).

Referring to claims 1-3 and 26, Maeda et al. disclose a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, each comprising a light-emitting diode chip and a luminescence conversion element, which converts the wavelength of at least part of an electromagnetic radiation emitted by the light-emitting diode chip, where a layer composite with a light-emitting diode layer sequence is applied to a carrier substrate for the plurality of light-emitting diode chips; producing a plurality of trenches in the layer composite (FIG. 57; col. 22, lines 21-36; col. 65, lines 26-45), inserting the layer composite into a cavity of a mold (117), driving a molding

compound (118), containing a luminescence conversion material (119), into the cavity in such a way that the trenches are at least partly filled with the molding compound (118), removing the mold (117), and separating the light-emitting diode light sources from the layer composite (FIG.15(a) & (b); col. 43, lines 1-55). Maeda et al. disclose the layer composite is a wafer composite of light-emitting diode chips (FIG. 57; col. 65, lines 26-45).

Referring to claim 9, side flanks (104) of at least some light-emitting diode chips are formed in such a way that pads of them do not run at right angles to front or rear surface of the light-emitting diode chips (FIG. 13(b); col. 41, lines 6-16).

Referring to claim 10, the side flanks (104) of at least some of the light-emitting diode chips are formed in such a way that pads of them run obliquely with respect to the perpendicular to front or rear surfaces of the light-emitting diode chips, curved or stepped (IFG. 13(b); col. 42, lines 6-16).

Referring to claim 11, the molding compound is a transfer molding compound and the mold is a transfer mold (Fig. 15(a) & (b); col. 43, lines 1-26).

Referring to claim 21, the position and color locus of the light-emitting diode light sources are subsequently determined and registered and the light-emitting diode light sources are subsequently sorted in accordance with their color locus (col. 33, lines 12-44).

Referring to claim 22, mounting the light-emitting diode light sources on a leadframe (5) and subsequently encapsulated in a translucent or transparent material (7) (FIG. 2; col. 21, lines 31-49).

Referring to claim 23, mounting the light-emitting diode light sources are mounted on a pre-housed leadframe (5) and covered with a translucent or transparent potting compound (7) (FIG. 2; col. 21, lines 31-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. in view of Uemura et al. (6,861,281).

Maeda et al. disclose the subject matter claimed above except the trenches formed along dividing lines between regions of adjacent light-emitting diode chips in the layer composite.

Uemura et al. disclose a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, each comprising a light-emitting diode chip where a layer composite with a light-emitting diode layer sequence is applied to a carrier substrate for the plurality of light-emitting diode chips (col. 6, lines 3-51); producing a plurality of trenches in the layer composite (col. 6, lines 52-59), and separating the light-emitting diode light sources (col. 7, lines 44-49; col. 8, lines 4-23).

Since Maeda et al. and Uemura et al. are both from the same field of endeavor, a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, the purpose disclosed by Uemura et al. would have been recognized in the pertinent art of Maeda et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maeda et al. by the trenches formed along dividing lines between regions of adjacent light-emitting diode chips in the layer composite as taught by Uemura et al. to improve productivity (col. 1, lines 37-50).

Referring to claim 4, Uemura et al. disclose the trenches formed along dividing lines between regions of adjacent light-emitting diode chips in the layer composite (col. 3; col. 8, lines 4-23).

Referring to claim 6, Uemura et al. disclose the inner walls of at least some of the trenches are formed in such a way that parts of the bottom surfaces do not run parallel with, and/or pads of the side walls do not run at right angles to, front or rear surfaces of the light-emitting diode chips (Fig. 3; col. 8, lines 8-24).

Referring to claim 7, Uemura et al. disclose the bottom surfaces of at least some of the trenches are formed so as to be V-shaped, convex, concave or stepped, and at least part of the light is coupled out of the light-emitting diode chips via the bottom surfaces of the trenches (Fig. 3; col. 8, lines 8-24).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. in view of Durocher et al. (6,614,103).

Maeda et al. discloses the subject matter claimed above except the carrier being flexible.

Durocher et al. disclose a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind where a plurality of light-emitting diode chips (59) are applied to a common carrier (31) in a regular arrangement; driving a molding compound (65), containing a luminescence conversion material; and separating the light-emitting diode light sources (fig. 9; col. 7, lines 23-29; col. 8, lines 42-48). Durocher et al. further disclose the carrier as flexible (col. 4, line 63 thru col. 5, line 3).

Since Maeda et al. and Durocher et al. are both from the same field of endeavor, a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, the purpose disclosed by Durocher et al. would have been recognized in the pertinent art of Maeda et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maeda et al. by the carrier being flexible as taught by Durocher et al. to be able to easily into a variety of lighting products (col. 3, lines 17-30).

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. in view of Gibb et al. (6,787,435).

Maeda et al. disclose the subject matter claimed above except producing the trenches by sawing and separating the light-emitting diode light sources by sawing.

Gibb et al. disclose a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind where a plurality of light-emitting diode chips are applied to a common carrier in a regular arrangement, and separating the light-emitting diode light sources (Fig. 3; col. 6, line 11 thru col. 8, line 28). Gibb et al. further disclose producing the trenches by sawing and separating the light-emitting diode light sources by sawing (col. 8, lines 13-20).

Since Maeda et al. and Gibb et al. are both from the same field of endeavor, a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, the purpose disclosed by Gibb et al. would have been recognized in the pertinent art of Maeda et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maeda et al. by producing the trenches by sawing and separating the light-emitting diode light sources by sawing as taught by Gibb et al. to improve device yield (col. 8, lines 13-20).

Allowable Subject Matter

Claims 13-20, 24 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: referring to claims 13,14, 19 and 24, prior art does not anticipate, teach, or suggest in which the cavity is formed in such a way that the inner walls

of the mold rest on the front and the rear of the layer composite respectively the chips.

Referring to claims 15 and 25, prior art does not anticipate, teach, or suggest in which the layer composite has electrical contact areas on the front side, to which, before the insertion of the layer composite into the cavity, an electrical connecting material with an approximately constant height is applied.

Referring to claim 16, prior art does not anticipate, teach, or suggest in which molding compound by which electrical contacts are covered is removed by thinning, at least until the electrical connecting material is exposed.

Referring to claims 17, prior art does not anticipate, teach, or suggest in which molding compound applied to the front is thinned at least until covered electrical connecting material is exposed, and in which the color locus (CIE color chart) of the light-emitting diode light sources is measured repeatedly and thus set specifically by means of further thinning.

Referring to claim 18, prior art does not anticipate, teach, or suggest in which electrical contact areas of the layer composite or of the light-emitting diode chips are sealed off before they are inserted into the cavity and exposed again before being separated.

Referring to claim 20, prior art does not anticipate, teach, or suggest in which the electrical contact are of the chips are sealed off by a front and/or rear inner wall of the mold, which comprise pad plates fitted such that they can move, which are pressed individually against the front and/or rear of the layer composite or the light-emitting diode chips.

Response to Arguments

Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fujisaki et al. (JP 62-004380) disclose a process for simultaneously producing a plurality of light-emitting diode light sources of the same kind, each comprising a light-emitting diode chip and a luminescence conversion element, which converts the wavelength of at least part of an electromagnetic radiation emitted by the light-emitting diode chip, where a layer composite with a light-emitting diode layer sequence is applied to a carrier substrate for the plurality of light-emitting diode chips; inserting the layer composite into a cavity of a mold, driving a molding compound, containing a luminescence conversion material, into the cavity in such a way that the trenches are at least partly filled with the molding compound, removing the mold, and separating the light-emitting diode light sources from the layer composite.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
30 May 2006

Zandra V. Smith
Supervisory Patent Examiner
30 May 2006